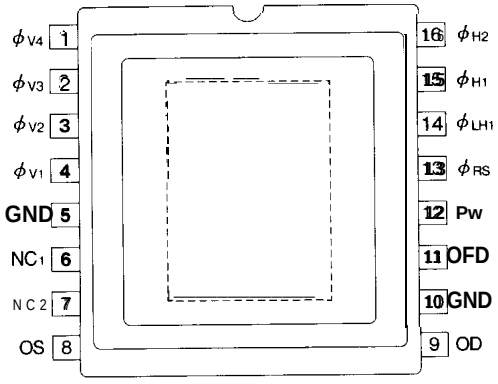
LZ2354AJ 1/3 type B/W CCD Area Sensor for EIA

DESCRIPTION

LZ2354J is a 1/3-type (6.0 mm) solid-state image sensor that consists of PN phote-diodes and CCDS (charge-coupled devices). Having approximately 410000 pixels (horizontal 811 X vertical 507), the sensor provides a high resolution stable B/W image.

PIN CONNECTIONS

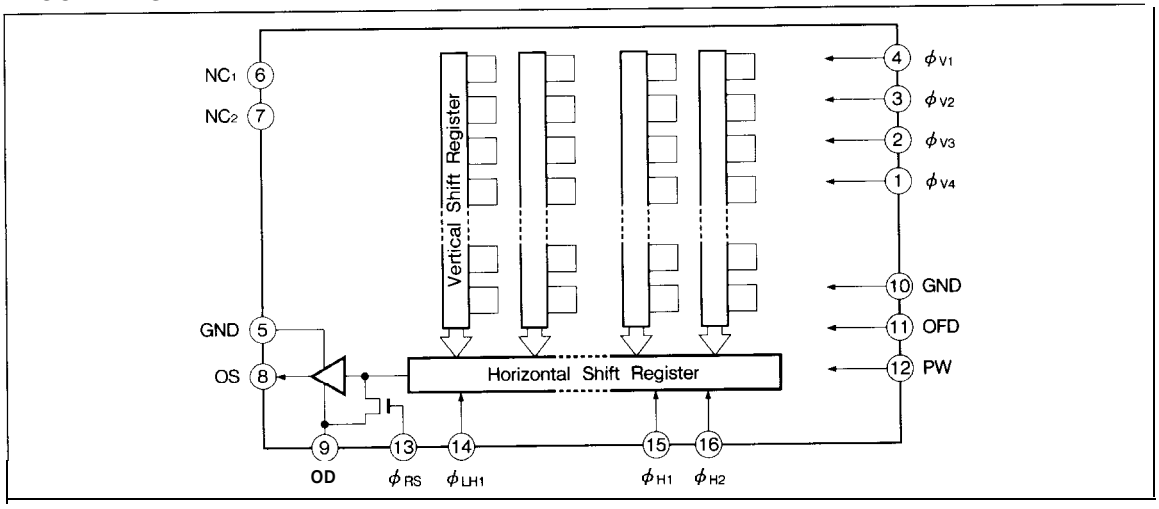
16-PfN SDIP TOP VIEW



FEATURES

- Number of pixels : 768 (H) × 494 (V)
  Pixel pitch : 6.4 μm (H) × 7.5 μm (V)
  Number of optical black pixels
  : Horizontal; front 3 and rear 40
  Vertical; front 11 and rear 2
- Low fixed pattern noise and lag
- No burn-in and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Variable electronic shutter (1/60 to 1/1 O 000 s)
- Compatible with EIA standard
- Package : 16-pin SDIPICERDIP](WDIPO1 6-N-0450)

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
OD	Output transistor drain
0 S	Video output
ϕ_{RS}	Reset transistor clock
$\phi_{V1}, \phi_{V2}, \phi_{V3}, \phi_{V4}$	Vertical shift register clock
ϕ_{H1}, ϕ_{H2}	Horizontal shift register clock
ϕ_{LH1}	Horizontal shift register final stage clock
OFD	Overflow drain
PW	P type well
GND	Ground
NC I NC2	No connection

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Output transistor drain voltage	V_{OD}	0 to +18	V	
Reset gate clock voltage	$V_{\phi RS}$	−0.3 to +18	V	
Vertical shift register clock voltage	$V_{\phi V}$	V_{PW} to +18	V	
Horizontal shift register clock voltage	$V_{\phi H}$	−0.3 to +18	V	
Horizontal shift register final stage clock voltage	$V_{\phi LH}$	−0.3 to +18	V	
Overflow drain voltage	V_{OFD}	o to +55	V	
Voltage difference between PW and vertical clock	$V_{PW} - V_{\phi V}$	−28 to O	V	1
Storage temperature	Tsta	−40 to +80	°C	
Operating ambient temperature	Topr	−20 to +70	°C	

NOTE :

1. The OFD clock ϕ_{OFD} is excluded

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Operating ambient temperature		Topr		25.0		℃	
Output transistor drain voltage		Voo	14.5	15.0	16.0	V	
Overflow drain voltage	When DC is applied	VOFD	5.0		19,0	V	1
	When pulse is applied p-p level	$V_{\phi OFD}$	23,0			V	2
Ground		GND		0.0		V	
P-well voltage		VPW	−10.0		$V_{\phi VL}$	V	
Vertical shift register clock	LOW level	$V_{\phi V1L}$, $V_{\phi V3L}$ $V_{\phi V2L}$, $V_{\phi V4L}$	−9.5	−9.0	−8.5	V	
	INTERMEDIATE level	$V_{\phi V1I}$, $V_{\phi V3I}$ $V_{\phi V2I}$, $V_{\phi V4I}$		0.0		V	
	HIGH level	$V_{\phi V1H}$, $V_{\phi V3H}$	16.0	16.5	17.0	V	
Horizontal shift register clock	LOW level	$V_{\phi H1L}$, $V_{\phi H2L}$	−0.05	0.0	0.05	V	
	HIGH level	$V_{\phi H1H}$, $V_{\phi H2H}$	4.7	5.0	6.0	V	
Horizontal shift register final stage clock	LOW level	$V_{\phi LH1L}$	−0.05	0.0	0,05	V	
	HIGH level	$V_{\phi LH1H}$	4.7	5.0	6.0	V	
Reset gate clock	LOW level	$V_{\phi RSL}$	0.0		VOD−11.(	V	
	HIGH level	$V_{\phi RSH}$	VOD−6.5		10.0	V	
Vertical shift register clink frequency		$f_{\phi V1}$, $f_{\phi V2}$ $f_{\phi V3}$, $f_{\phi V4}$		15.73		kHz	
Horizontal shift register clock frequency		$f_{\phi H1}$, $f_{\phi H2}$ $f_{\phi LH1}$		14.32		MHz	
Reset gate clock frequency		$f_{\phi RS}$		14.32		MHz	

∗ Connect NC1 and NC2 to GND directly or through a capacitor lager than 0,047 μF

NOTES :

1. When DC voltage is applied, shutter spaed is 1/60 seconds.
2. When pulse is applied, shutter spaed is lees than 1/60 seconds.

ELECTRICAL CHARACTERISTICS (Drive method : Field Accumulation)

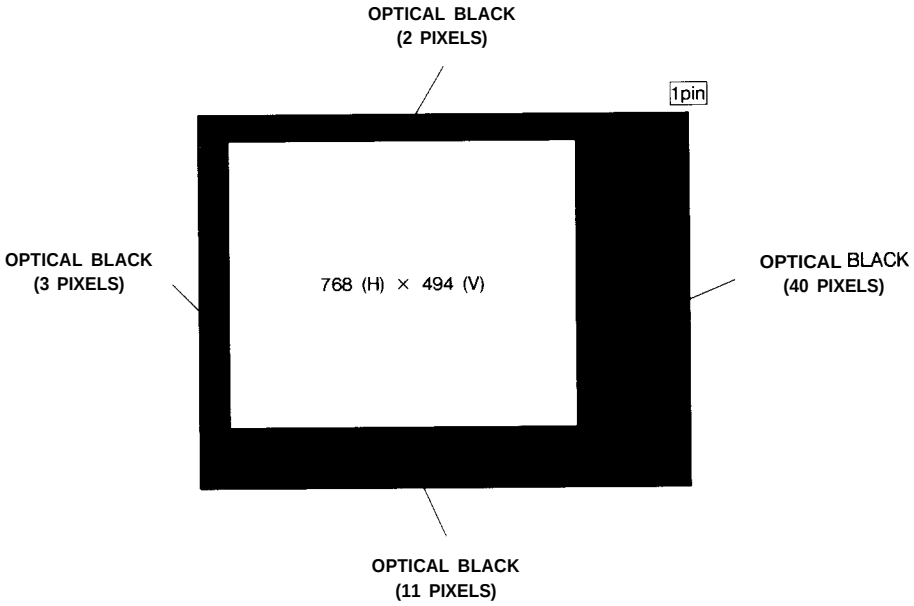
(Ta = 25°C, Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mmt))

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Standard output voltage	Vo		150		mV	2
Photo response non-uniformity	PRNU			10	%	3, 4
Saturation output voltage	Vsat	700			mV	3, 5
Dark output voltage	Vdark		0,5	3.0	mV	1, 6
Dark signal non-uniformity	DSNU		0.5	2.0	mV	1, 3, 7
Sensitivity	R	320	450		mV	6
Gamma	Y		1			
Smear ratio	SMR		– 75	– 70	dB	9, 10
Image lag	AI			1,0	0/0	11
Blooming suppression ratio	ABL	1000				9, 12
Output transistor drain current	100		4,0	8.0	mA	
Output impedance	Ro		350		Ω	
Dark noise	Vnoise		0.2	0.3	mV	13
OB difference in level				1.0	mV	1, 14

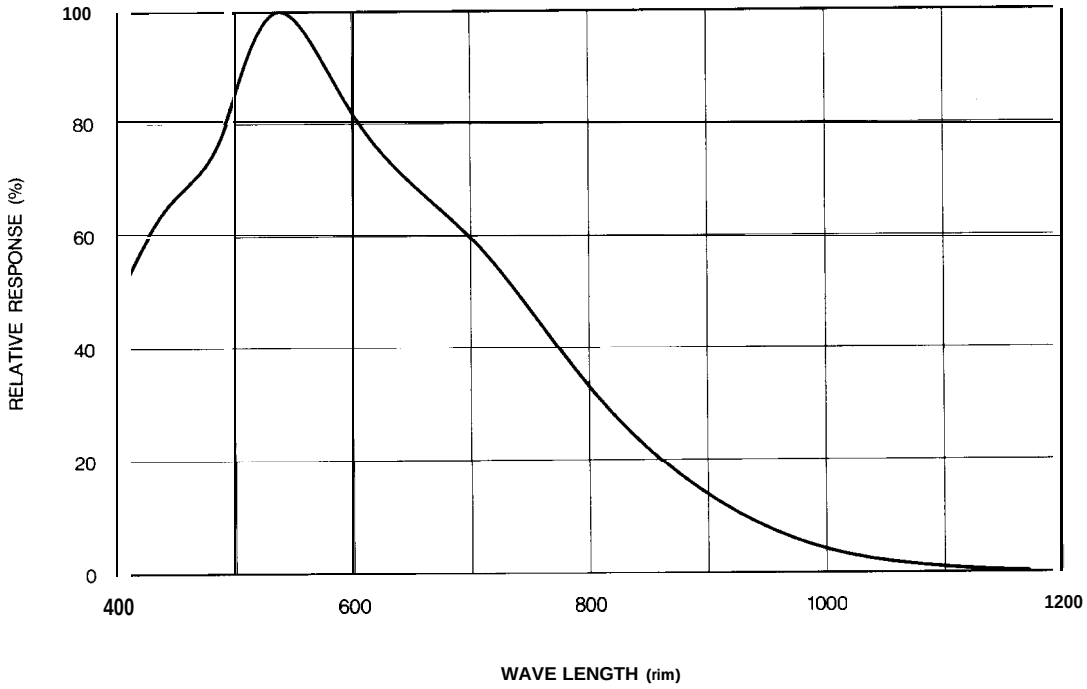
NOTES :

1. Ta : +60°C
2. The average output voltage under the uniform i Illumination. The standard exposure condition is defined when Vo is 150 mV.
3. The image area is divided into 10X 10 segments. The segment's voltage is the average output voltage of all the pixels within the segment.
4. PRNU is defined by (Vmax – Vmin)/Vo, where Vmax and Vmin are the maximum and the minimum values of each segment's voltage respectively, under the stand ard exposure condition.
5. The minimum segment's voltage under 10 times exposure of the standard exposure condition.
6. The average output voltage under the non-exposure condition.
7. DSNU is defined by (Vdmax – Vdmin), where Vdmax and Vdmin are the maximum and the minmum values of each segment's voltage respectively, under the non-exposure condition.
8. The average output voltage when a 1000 lux light source with a 90% reflector is imaged with a lens at F4, f50 mm.
9. The sensor is exposed only in the central area of V/l O square, where V is the vertical image size.
10. SMR is defined by the ratio of the smear voltage detected during the vertical blanking period to the maximum output voltage in the V/l O square, with a lens at F4.
11. The sensor is exposed at the exposure level corresponding to the standard condition. Al is defined by the ratio of the lag voltage measured at the 1st field during the non-exposure period to the standard output voltage.
12. ABL is defined by the ratio of the exposure at the standard condition to the exposure at a point where a blooming is observed.
13. The RMS value of the dark noise after CDS, The bandwidth range is from 100 kHz to 4,2 MHz. SC trap on.
14. The difference of the average output voltage between the effective area and the OB area under the non-exposure condition.

PIXEL STRUCTURE



SPECTRAL RESPONSE EXAMPLE

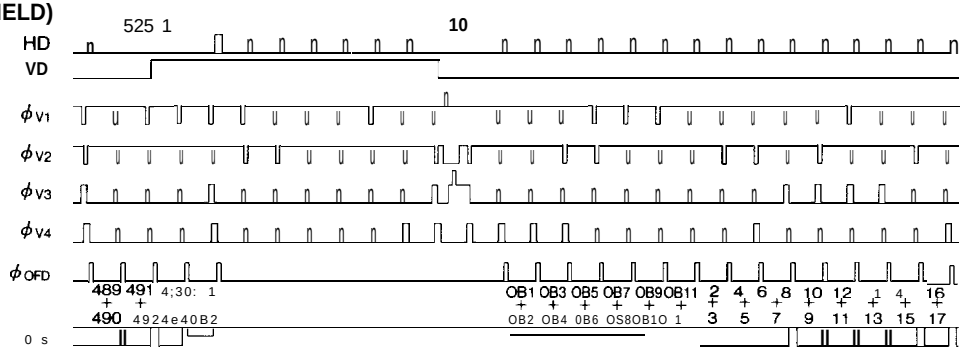


TIMING DIAGRAM EXAMPLE

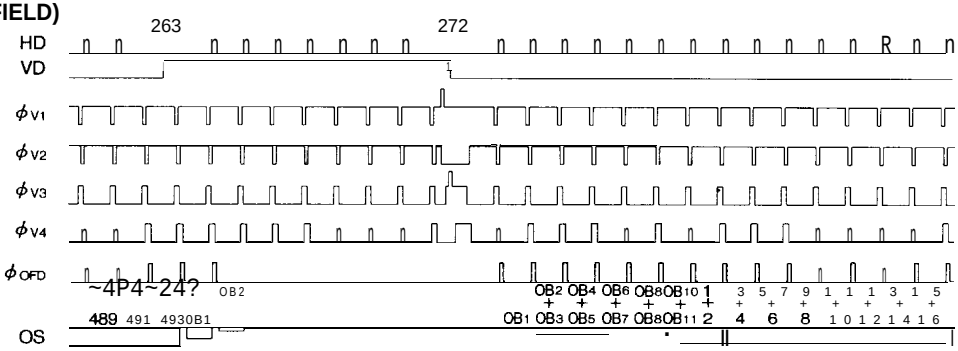
VERTICAL TRANSFER TIMING

Shutter speed 1/2000 s

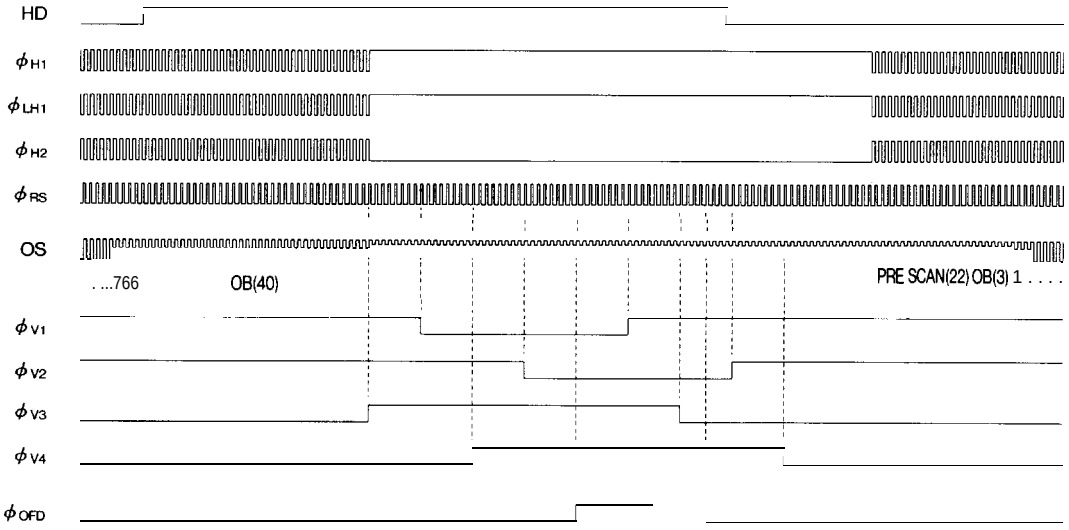
(ODD FIELD)



(EVEN FIELD)

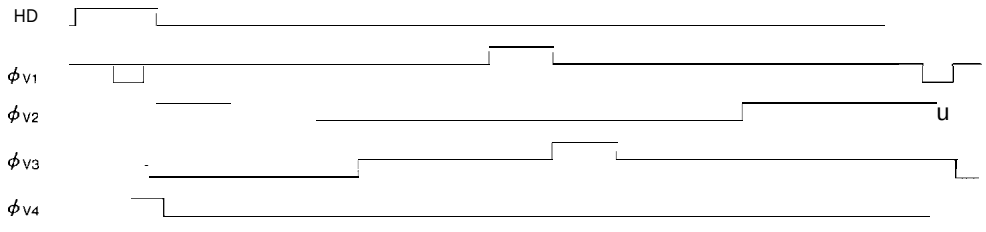


HORIZONTAL TRANSFER TIMING

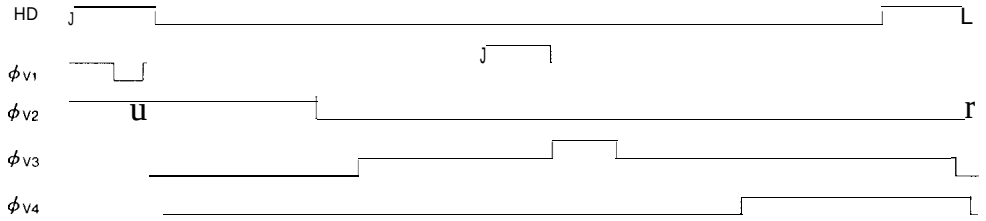


READOUT TIMING

(ODD FIELD)



(EVEN FIELD)



SYSTEM CONFIGURATION EXAMPLE